REMARKS

Regarding the specification: The specification has been amended in direct response to the Examiner's comments. Specifically, item 602 in Figure 6 is now identified in the specification. Decoder 602 corresponds in displayed structure and relative connection to the apparently similar decoder 502 used in the embodiment shown in Figure 5A, the decoders of which are discussed at least at page 16, lines 26-28. Also, responsive to the Examiner's inquiry, Applicants note that the programmability of the partitioning of the register file, and some elements which may be used to implement same, are discussed at least at page 19, line 26 through page 20, line 17, et seq. where the programmable addressing scheme is discussed.

Regarding the drawings: A "proposed drawing correction" to Figures 1, 5A and 6 has been provided in direct response to the Examiner's request. Specifically, Figure 1 has been amended to identify memory controller 102, UPA controller 116 and PCI controller 120, all of which are discussed in the specification at least at page 6, line 19 through page 7, line 24, et. seq. Figure 5A has been amended to identify decoder 502 which is discussed in the specification at least at page 16, lines 26-28. Figure 6 has been amended to identify decoder 602 which is discussed in the specification as amended herein.

Regarding the claims: Claims 1-28 are pending and stand rejected. Claims 1, 15 and 23 have been amended. Support for the amendments may be found at least in Figures 7, 8A and 8B and in the corresponding descriptive text in the specification. No new matter has been added.

Claims 1, 3-14 and 23-28 stand rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 5,592,679 (hereinafter, Yung) in view of U.S. Patent No. 5,911,149 (hereinafter, Luan). Claims 2 and 15-22 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Yung in view of Luan and further in view of U.S. Patent No. 6,023,757 (hereinafter, Nishimoto).

Regarding independent claim 1, Yung and Luan do not disclose, alone or in combination, a processor including "a substantially contiguous register file that is divided into a plurality of register file segments" which are further "partitioned into global registers and local registers," much less such a processor in which the "global registers and the...local registers are

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programmably configurable," all as required by independent claim 1. For example, although Yung discloses a global register file/memory 290 separate from execution units 241 and a number of local register buffers 241d in each execution unit 241, Yung and Luan do not disclose, alone or in combination, "a *register file* that is divided into a plurality of *register file segments*...partitioned into *global registers* and *local registers*," all as required by independent claim 1 (emphasis added). The claimed hierarchy is not taught. Therefore, independent claim 1 is allowable over Yung and Luan for at least this reason.

Regarding independent claim 15, Yung, Luan and Nishimoto do not disclose, alone or in any combination, a processor including "a substantially contiguous register file...divided into a plurality of register file segments...including a plurality of registers that are partitioned into global registers and local registers," all as required by independent claim 15. For example, although Yung discloses a global register file/memory 290 separate from execution units 241 and a number of local register buffers 241d in each execution unit 241, Yung, Luan and Nishimoto do not disclose, alone or in any combination, "a *register file*...divided into a plurality of *register file segments*...including a plurality of registers that are partitioned into *global registers* and *local registers*," all as required by independent claim 15 (emphasis added). Therefore, independent claim 15 is allowable over Yung, Luan and Nishimoto for at least this reason.

Regarding independent claim 23, Yung and Luan do not disclose, alone or in combination, a method of operating a processor including "a substantially contiguous register file divided into a plurality of register file segments" and "partitioning the register file segments into global registers and local registers," much less such a method including "programmably partitioning the register file so that the number of global registers and the number of the local registers are selectable and variable," all as required by independent claim 23. For example, although Yung discloses a global register file/memory 290 separate from execution units 241 and a number of local register buffers 241d in each execution unit 241, Yung and Luan do not disclose, alone or in combination, "a *register file* divided into a plurality of *register file segments*" much less "partitioning the *register file segments* into *global registers* and *local registers*," all as required by independent claim 23 (emphasis added). Therefore, independent claim 23 is allowable over Yung and Luan for at least this reason.

Each of independent claims 1, 15 and 23 are allowable over the corresponding cited references for at least the above reasons. Claims 2-14 depend from claim 1 and are allowable for at least this reason. Claims 16-22 depend from claim 15 and are allowable for at least this reason. Claims 24-28 depend from claim 23 and are allowable for at least this reason.
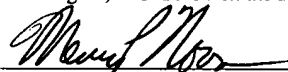
Conclusion

Claims 1-28 remain pending in the application. The rejection of claims 1-28 under 35 U.S.C. 103(a) as being unpatentable over Yung in view of Luan, and sometimes further in view of Nishimoto has been responded to in part by traversal and in part by amendment.

In view of the amendments and remarks set forth herein, and in view of the remarks previously offered by Applicants in prior submissions, which are hereby incorporated by reference herein and reasserted, Applicants believe the application and claims are in condition for allowance and a notice to that effect is solicited. Nonetheless, should any issues remain that might be amenable to resolution through a telephonic interview, the Examiner is requested to telephone the undersigned.

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CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to Commissioner for Patents, Washington, D.C. 20231 on the date shown below.

Michael P. Noonan   _March 18, 2003_
Michael P. Noonan   Date

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Respectfully submitted,

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